UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,212	05/18/2001	Kozo Nakamura	82821	6761

7590 05/06/2003

Welsh & Katz
22nd Floor
120 South Riverside Plaza
Chicago, IL 60606-3913

EXAMINER
SONG, MATTHEW J

ART UNIT	PAPER NUMBER
1765	13

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/856,212	NAKAMURA ET AL.
	Examiner	Art Unit
	Matthew J Song	1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7 and 9-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7 and 9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other

DETAILED ACTION

Claim Objections

1. Claim 7 recites the limitation "the control section" in the last line. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-5 and 9-11 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 recites, "a method for producing a **relatively defect free** silicon single crystal". There is no support for this limitation in the instant specification for forming a "relatively defect free" crystal. The instant specification states forming a "perfect crystal", not a relatively defect free crystal on page 29 using the claimed parameters, likewise for claims 2-5 and 9-11.

4. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claimed control means is not taught in the instant specification. On page

14, line 22 thru page 15, line 8, the ingot production device is taught. However, there is no teaching of the control means, merely adjusting the shield element **25** and changing the shield amount.

5. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 7 recites, "moving the heat shielding element on the basis of an instruction from the control section". There is no support for a control section in the instant specification on page 14, line 22 thru page 15, line 8.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7 Claims 1-5 and 9-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 recites, "a method for producing a **relatively defect free** silicon single crystal". The term "relatively" is indefinite. It is unclear the quantity of defects, which are permissible for a single crystal to be relatively defect free. In other words, it is unclear what the difference is between "relatively defect free" and defect rich.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 1 and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al (US 5,968,264).

Iida et al teaches a single crystal ingot of silicon was pulled while varying the average pulling rate over a range of 1.0 mm/min and 0.4 mm/min. Iida et al also teaches the temperature gradient in an in-crystal descending temperature zone between a melting point of silicon and 1400°C in the vicinity of the solid-liquid interface was set as follows: G_e=45.0°C/cm and G_c=42.0 °C/cm, where G_e reads on applicant's G outer and G_c reads on applicant's G center. The ratio of G_e/G_c can be determined to 1.07 and at a pulling rate of 0.72 mm/min the V/G at the center is 0.16 mm^2/°C*min and at the outer periphery is 0.17 mm^2/°C*min (col 14, ln 20-67).

Iida does not teach temperature gradient in a pulling axis direction within a temperature range from silicon melting point to 1350°C. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Iida by attempting to optimize the temperature range by conducting routine experimentation.

Referring to claim 4, Iida et al is silent to a silicon wafer with decreased grown-in defects, this reads on applicant's relatively defect free, which is obtained from the silicon ingot of claim 1. It is inherent to Iida's invention to produce a silicon wafer with decreased grown-in defects because Iida teaches similar growth conditions of a silicon single crystal ingot as applicant.

Referring to claim 5, Iida et al is silent to a silicon perfect single crystal wafer free from grown-in defects obtained from the silicon ingot of claim 1. It is inherent to Iida's invention to produce a silicon wafer with decreased grown-in defects because Iida teaches similar growth conditions of a silicon single crystal ingot as applicant.

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al (US 5,968,264) in view of Luter et al. (US 5,922,127).

Iida et al teaches all of the limitations of claim 2, except the conditions (a) and (b) of claim 1 are adjusted by changing a distance between a heat shielding element equipped in a Czochralski method-based silicon single crystal production device and silicon melt.

In an apparatus for pulling single crystals, Luter et al teaches a crucible mounted on a motorized turntable which raises the crucible to maintain the surface of the molten source material at a constant level as the ingot grows and the source material is removed from the melt (col 3, ln 60-65). Luter et al also teaches a heat shield (40) mounted above the upper surface of the molten source material (col 4, ln 32-37). Luter et al discloses the a heat shield may be positioned within the crucible above the melt for conserving heat at the interface between the ingot and molten material to prevent heat loss from the melt surface, which reduces the instantaneous axial thermal gradient G_o (col 2, ln 15-25), therefore Luter reads on applicant's limitation of adjusting conditions by changing the distance between a heat shielding element and the silicon melt. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Iida et al with Luter to avoid undesired changes in the thermal profile during the growth process.

11. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hourai et al (US 5,954,873).

Hourai et al teaches the relationship of V/G and the position in the radial direction of the crystal in Fig 2, where V is the single crystal pulling rate (mm/min) and the inside-crystal temperature gradient in the direction of the pulling axis in a high temperature zone from the melting point of silicon to 1300°C. Hourai et al also teaches the single crystal pulling rate and the inside-crystal temperature gradient in the axial direction are two critical parameters for controlling the diameter of an oxidation-induced stacking fault (OSF) ring and the diameter of the OSF ring can be determined by the ratio of V/G (col 4, ln 50-60). Hourai discloses to compensate for changes in the temperature gradient of the crystal, the pulling rate is adjusted so that a constant V/G may be achieved (col 6, ln 55-60)

Hourai does not teach the parameter of a V/G=0.16-0.18 $mm^2/°C*min$ or a G outer/G center $\leq$ 1.10. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Hourai by deriving the condition of claim 1, based on the profile of Fig 2.

Hourai does not teach temperature gradient in a pulling axis direction within a temperature range from silicon melting point to 1350°C It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Hourai by attempting to optimize the temperature range by conducting routine experimentation.

Hourai is silent to a relatively defect free silicon wafer, however this is inherent to Hourai et al because Hourai et al teaches similar pulling conditions, as applicant.

Referring claim 3, Hourai discloses to compensate for changes in the temperature gradient of the crystal, the pulling rate is adjusted so that a constant V/G may be achieved (col 6, ln 55-60).

Referring to claim 4, Hourai et al is silent to a silicon wafer with decreased grown-in defects, which is obtained from the silicon ingot of claim 1. It is inherent to Hourai's invention to produce a silicon wafer with decreased grown-in defects because Hourai teaches similar growth conditions of a silicon single crystal ingot as applicant.

Referring to claim 5, Hourai et al is silent to a silicon perfect single crystal wafer free from grown-in defects obtained from the silicon ingot of claim 1. It is inherent to Hourai's invention to produce a silicon wafer with decreased grown-in defects because Hourai teaches similar growth conditions of a silicon single crystal ingot as applicant.

12. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 5,942,032) in view of Luter (5,922,127).

Kim et al teaches a heat shield assembly for use in a crystal puller of the type used to grow monocrystalline silicon ingots according to the Czochralski method. Kim et al also teaches a crystal puller (12) includes a shell for isolating an interior, which includes a lower crystal growth chamber, this reads on applicant's limitation of a closed container. Kim et al discloses a quartz crucible containing a molten semiconductor source, where the crucible is mounted on a turntable for rotation about a vertical axis and is capable of being raised with the growth chamber. Kim et al also discloses heating panels (24) heat the crucible (col 4, 42-67). Kim et al also teaches the heat shield assembly an intermediate heat shield (40), a lower heat shield (42)

and an upper heat shield (36) (col 5, ln 15-65) and the heat shield assembly can be raised and lowered using the existing pulling mechanism of the crystal puller (12) (col 3, ln 15-20). Kim et al discloses the upper heat shield is positioned so that the portions of the ingot entering the upper heat shield are approximately at 1150°C and inside the upper heat shield, heat transfer from the ingot to the sidewalls is reduced so that the instantaneous axial temperature gradient G_o is lessened in the portion of the upper heat shield (col 9, ln 40-50 and ln 25-27). Kim et al also discloses the lower heat shield prevents heat from radiating from the sidewalls of the crucible to the ingot (col 9, ln 15-22). Kim et al also discloses using the heat assembly (10) a high v/G_o ratio is achieved and the ratio of v/G_o is increased without changing the pull rate v, however variation in the pull rate may be employed to increase the v/G_o ratio (col 9, ln 55-67 and col 10, ln 1-10). Kim et al also discloses a winch, this reads on applicant's drive mechanism, is activated to move the heat shield assembly **10** and a switch is proved in the growth chamber to shut off the winch when the heat shield assembly is fully raised (col 8, ln 1-67)

Kim et al does not teach a pulling element for pulling a silicon single crystal ingot, while rotating.

In a method of pulling a monocrystalline ingot used to manufacture semiconductor wafers, Luter et al discloses a pulling mechanism (30) rotates a seed crystal C and moves it up and down through the growth chamber (col 4, ln 5-10). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim with Luter because counter-rotating the crystal and crucible prevents the exchange of impurities between the melt directly below the crystal and the residual melt, note Chapter 2.5 of Zulehuler and Huber.

Referring to claim 7, the combination of Kim and Luter teach a heat shield assembly **10**, which controls the temperature gradient in a pulling axis direction, this reads on applicant's control means and a winch (col 8, ln 5), this reads on applicant's drive mechanism and switch, which instructs the drive mechanism to stop.

13. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi et al. (US 5,931,662) in view of Iida et al (US 5,968,264).

Adachi et al teaches the preferred annealing conditions for forming defect-free region, where defect-free reads on applicant's perfect crystal, is to ramp up to a temperature in excess of 1100°C and annealing preformed at temperatures ranging from 500°C to 900°C for more than 10 minutes can provide IG functions by forming oxide precipitates, BMD. Adachi et al also teaches BMD for IG functions can also be formed by ramping up from 500°C to 900°C at a rate of 0.5°C/min (col 10, ln 60-67). Adachi et al discloses maintaining a temperature between 500°C to 900°C for more than 10 minutes during the ramp down process following sustained heating at a temperature in excess of 1100°C makes it possible to provide IG functions by forming BMD at a rate of 0.5°C/min (col 11, ln 5-15). Adachi et al also discloses silicon single crystal wafers were loaded into an annealing boat and into a furnace pre-heated to 700°C (col 11, ln 50-60). Adachi teaches in Fig 11 and 12 indicating the relationship between surface depth and oxygen concentration and the results indicate DZ layers had been secured in all wafers after annealing(col 12, ln 46-55)

Adachi et al does not teach the single crystal wafer is relatively defect free.

In a method of forming a single crystal wafer, Iida et al teaches a method of forming a single crystal wafer with very few crystal defects, this reads on applicant's relatively defect free wafer, and when this wafer undergoes an oxygen precipitation heat treatment and is observed by means of X rays, uniform precipitation contrast is observed over the surface thereof and a small number of striation rings is observed (col 13, ln50 to col 14, ln 15). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Adachi et al with Iida et al's silicon wafer to form a uniform precipitation.

The combination of Adachi et al and Iida et al does not teach a heat treatment temperature at the initial entry of the silicon single crystal wafer to be a target of the heat treatment is 500°C or less. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Adachi by attempting to optimize same by conducting routine experimentation.

Referring to claim 10, the combination of Adachi et al and Iida et al is silent to a uniform distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment. It is inherent to the combination of Adachi et al and Iida et al's invention to uniform the distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment because the combination of Adachi et al and Iida et al teaches a similar heat treatment with an ultimate temperature set in a range of 500-900°C at a similar ramping rate of 0.5 °C/min as applicant.

Referring to claim 11, the combination of Adachi et al and Iida et al is silent to adjusting the distribution of an oxide precipitate density of the silicon single crystal wafer after the heat treatment. It is inherent to the combination of Adachi et al and Iida et al's invention to uniform

the distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment because the combination of Adachi et al and Iida et al teaches a similar heat treatment with an ultimate temperature set in a range of 700-900°C as applicant.

Referring to claim 12, Adachi teaches the oxygen concentration is less than $13x10^{17}$ atoms/cm^3 in the DZ layer in Figs 11 and 12. If Adachi does not teach this in Figs 11 and 12, then it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Adachi by attempting to optimize same by conducting routine experimentation.

Referring to claim 13, the combination of Adachi et al and Iida et al teaches silicon wafers were annealed under similar conditions as taught by applicant.

Response to Arguments

14. Applicant's arguments filed 9/9/2002 have been fully considered but they are not persuasive.

The arguments regarding the Iida et al reference concerning claims 1 and 4-5 are not deemed persuasive. Applicant's arguments are based on a single example taught in the Iida reference and is unduly limiting the reference. Varying other parameters of the growth such as crystal diameter, melt temperature, etc will inherently cause changes in the defect regions and those changes would be anticipated by a person of ordinary skill in the art at the time of the invention. The Iida reference teaches the key parameter is maintaining the difference in crystal gradient between the edge and center and is open to variations in the pulling speed to obtain a region with a reduced amount of defects. The Iida reference teaches all the parameters instantly claimed, as discussed previously in the rejection, except Iida et al teaches a melt temperature of

1420°C and differs from the claimed melt temperature of 1350°C. Such a difference in the temperature parameter would affect the properties of the grow crystal. Therefore, the optimum crystal pulling will inherently change and it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Iida by optimizing the pulling speed to produce a crystal with a reduced number of defects.

The arguments regarding the Hourai et al reference concerning claims 1 and 3-5 are not deemed persuasive. The instant specification states in the first full paragraph of page 13, "the present invention has an aspect where **more appropriate conditions** that the optimum conditions presented by Hourai et al are presented in the production process of a silicon single crystal". This is a teaching that the instantly claimed invention has merely optimized Hourai et al and optimization of result effective process parameters is held to be obvious (MPEP 2144.05). The inside crystal temperature gradient and pulling rate are taught by Hourai et al to be result effective variable, note column 4, lines 50-60.

Applicant's arguments over claim 7 have been considered but have not been found persuasive. The combination of Kim and Luter teach a heat shield assembly **10**, which controls the temperature gradient in a pulling axis direction, this reads on applicant's control means and a winch (col 8, ln 5), this reads on applicant's drive mechanism and switch, which instructs the drive mechanism to stop.

15. Applicant's arguments with respect to claims 9-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Von Ammon et al ("The dependence of bulk defects on the axial temperature gradient of silicon crystal during Czochralski growth") teaches the critical pulling rate varies with the crystal diameter and the type of heat shield (abstract).

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 703-305-4953. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin L Utech can be reached on 703-308-3868. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Matthew J Song
Examiner
Art Unit 1765

MJS
May 5, 2003